INTL9641 Product Brief

1. Description

The INTL9641 is a 2-to-1 I2C master demultiplexer with an arbiter function. It is designed for high reliability dual master I2C-bus applications where correct system operation is required, even when two I2C-bus masters issue their commands at the same time. The arbiter will select a winner and let it work uninterrupted, and the losing master will take control of the I2C-bus after the winner has finished. The arbiter also allows for queued requests where a master requests the downstream bus while the other master has control.

A race condition occurs when two masters try to access the downstream I2C-bus at almost the same time. The INTL9641 intelligently selects one winning master and the losing master gains control of the bus after the winning master gives up the bus or the reserve time has expired.

Multiple transactions can be done without interruption. The time needed for multiple transactions on the downstream bus can be reserved by programming the Reserve Time register. During the reserve time, the downstream bus cannot be lost.

Software reset allows a master to send a reset through the I2C-bus to put the INTL9641's registers into the power-on reset condition.

2. Features

- 2-to-1 bidirectional master selector
- Channel selection via I2C-bus
- I2C-bus interface logic; compatible with SMBus standards
- 2 active LOW interrupt outputs to master controllers
- Active LOW reset input
- Software reset
- Four address pins allowing up to 112 different addresses
- Arbitration active when two masters try to take the downstream I2C-bus at the same time
- The winning master controls the downstream bus until it is done, as long as it is within the reserve time
- Bus time-out after 100 ms on an inactive downstream I2C-bus (optional)
- Readable device ID (manufacturer, device type, and revision)
- Bus initialization/recovery function
- Low Ron switches
- Allows voltage level translation between 1.8 V, 2.3 V, 2.5 V, 3.3 V and 3.6 V buses
- No glitch on power-up
- Supports hot insertion

INTL9641 Product Brief

- Software identical for both masters
- Operating power supply voltage range of 2.3 V to 3.6 V
- All I/O pins are 3.6 V tolerant
- Up to 1 MHz clock frequency
- ESD protection exceeds 6000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating Temperature=-40°C to 85°C
- Packages offered: TSSOP16(5.00 mm x 4.40 mm)

3. Applications

- High reliability systems with dual masters
- Gatekeeper multiplexer on long single bus
- Bus initialization/recovery for slave devices without hardware reset
- Allows masters without arbitration logic to share resources

4. Functional Diagram

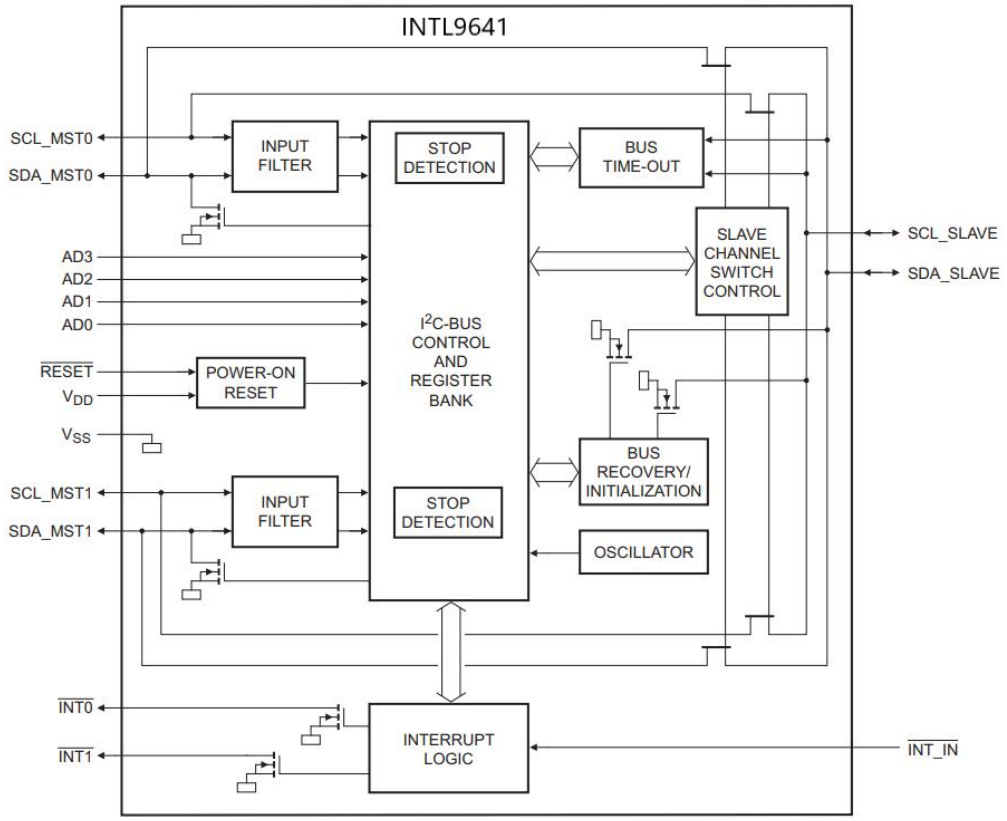

Figure 1 Functional Diagram